

74LVC3G17

Triple non-inverting Schmitt trigger with 5 V tolerant input

Rev. 05 — 13 March 2008

Product data sheet

1. General description

The 74LVC3G17 provides three non-inverting buffers with Schmitt trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC3G17 as a translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Applications

- Wave and pulse shapers for highly noisy environments

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC3G17DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC3G17DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC3G17GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC3G17GM	-40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLF based; body 1.6 × 1.6 × 0.5 mm	SOT902-1

5. Marking

Table 2. Marking codes

Type number	Marking code
74LVC3G17DP	V17
74LVC3G17DC	V17
74LVC3G17GT	V17
74LVC3G17GM	V17

6. Functional diagram

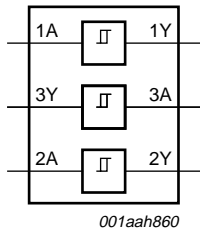


Fig 1. Logic symbol

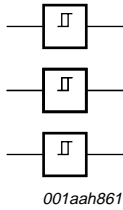


Fig 2. IEC logic symbol

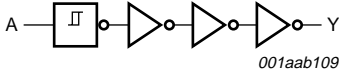
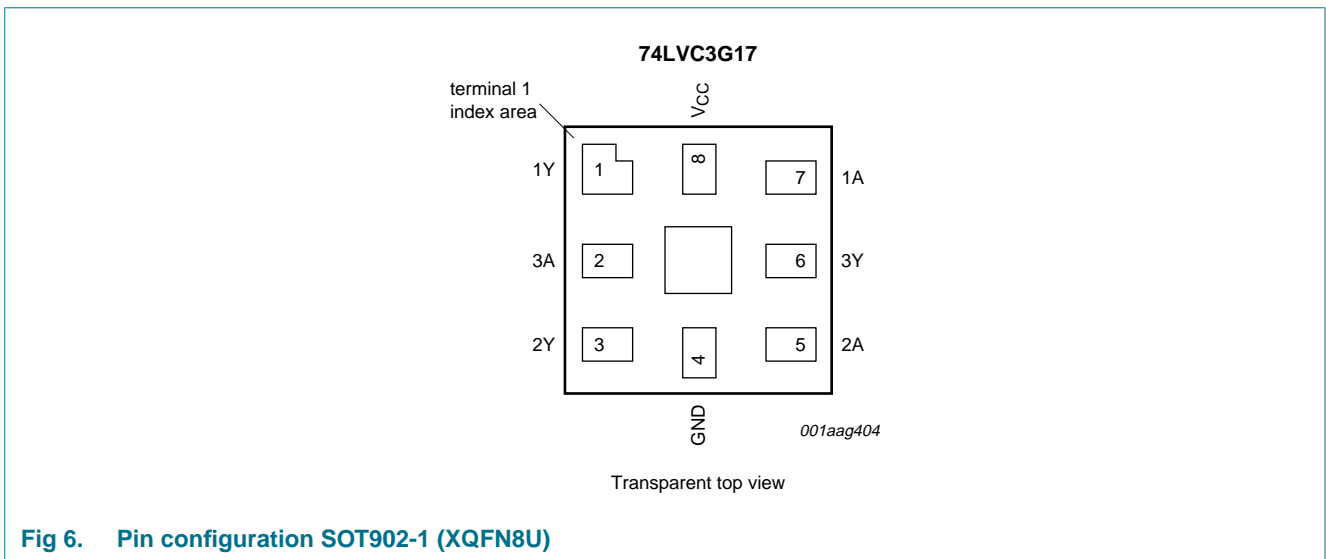
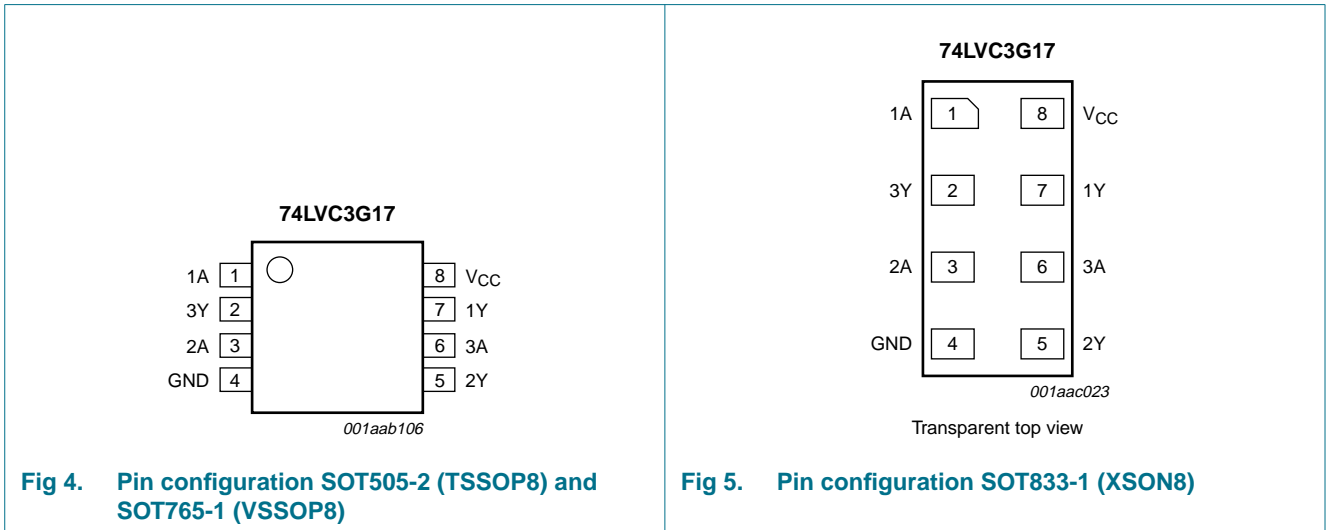


Fig 3. Logic diagram (one gate)

7. Pinning information

7.1 Pinning



7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1 and SOT833-1	SOT902-1	
1A	1	7	data input 1
3Y	2	6	data output 3
2A	3	5	data input 2
GND	4	4	ground (0 V)
2Y	5	3	data output 2
3A	6	2	data input 3
1Y	7	1	data output 1
V _{CC}	8	8	supply voltage

8. Functional description

Table 4. Function table^[1]

Input	Output
nA	nY
L	L
H	H

- [1] H = HIGH voltage level;
L = LOW voltage level.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		^[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	Active mode	^[1] -0.5	V _{CC} + 0.5	V
		Power-down mode	^{[1][2]} -0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[3] -	250	mW

- [1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- [2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

- [3] For TSSOP8 and VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8 and XQFN8U packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

10. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$						
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.45	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.55	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	-	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.9	-	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	-	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.3	-	-	V
		$I_O = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.8	-	-	V
I_I	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 0\text{ V to }5.5\text{ V}$	[2] -	± 0.1	± 5	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 5.5\text{ V}; V_{CC} = 0\text{ V}$	-	± 0.1	± 10	μA
I_{CC}	supply current	$V_I = 5.5\text{ V or GND}; I_O = 0\text{ A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	0.1	10	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6\text{ V}; I_O = 0\text{ A}; V_{CC} = 2.3\text{ V to }5.5\text{ V}$	[2] -	5	500	μA
C_I	input capacitance		-	3.5	-	pF
$T_{amb} = -40\text{ °C to }+125\text{ °C}$						
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.70	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.45	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.60	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.80	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.80	V

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.4	-	-	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±20	μA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	-	±20	μA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	-	40	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	-	5	mA

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] These typical values are measured at V_{CC} = 3.3 V.

12. Dynamic characteristics

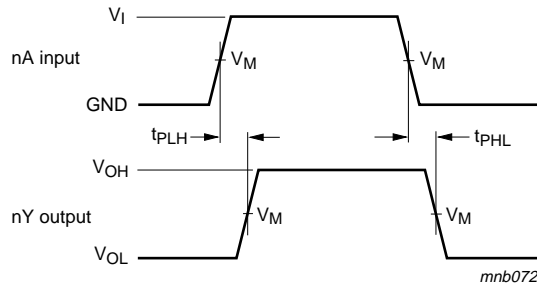
Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Figure 7 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.5	5.6	10.5	1.5	13.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.7	6.5	1.0	8.5	ns
		V _{CC} = 2.7 V	1.0	3.8	6.5	1.0	8.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.6	5.7	1.0	7.1	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	2.7	4.3	1.0	5.4	ns
C _{PD}	power dissipation capacitance	per buffer; V _{CC} = 3.3 V; V _I = GND to V _{CC} ^[3]	-	16.3	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of outputs.

13. Waveforms

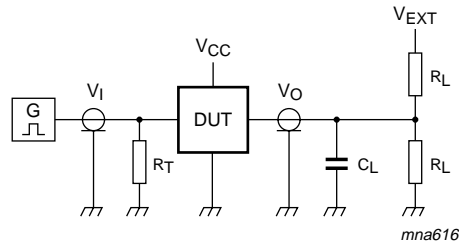


Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 7. The input (nA) to output (nY) propagation delays and the output transition times

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Load circuitry for switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

14. Transfer characteristics

Table 11. Transfer characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{T+}	positive-going threshold voltage	see Figure 9 and Figure 10						
		V _{CC} = 1.8 V	0.70	1.10	1.50	0.70	1.70	V
		V _{CC} = 2.3 V	1.00	1.40	1.80	1.00	2.00	V
		V _{CC} = 3.0 V	1.30	1.76	2.20	1.30	2.40	V
		V _{CC} = 4.5 V	1.90	2.47	3.10	1.90	3.30	V
V _{T-}	negative-going threshold voltage	see Figure 9 and Figure 10						
		V _{CC} = 1.8 V	0.25	0.61	0.90	0.25	1.10	V
		V _{CC} = 2.3 V	0.40	0.80	1.15	0.40	1.35	V
		V _{CC} = 3.0 V	0.60	1.04	1.50	0.60	1.70	V
		V _{CC} = 4.5 V	1.00	1.55	2.00	1.00	2.20	V
V _H	hysteresis voltage (V _{T+} - V _{T-}); see Figure 9 , Figure 10 and Figure 11	V _{CC} = 1.8 V	0.15	0.49	1.00	0.15	1.20	V
		V _{CC} = 2.3 V	0.25	0.60	1.10	0.25	1.30	V
		V _{CC} = 3.0 V	0.40	0.73	1.20	0.40	1.40	V
		V _{CC} = 4.5 V	0.60	0.92	1.50	0.60	1.70	V
		V _{CC} = 5.5 V	0.70	1.02	1.70	0.70	1.90	V

[1] All typical values are measured at T_{amb} = 25 °C.

15. Waveforms transfer characteristics

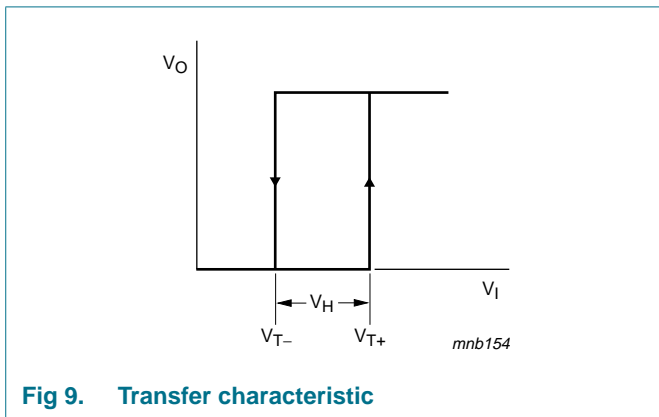


Fig 9. Transfer characteristic

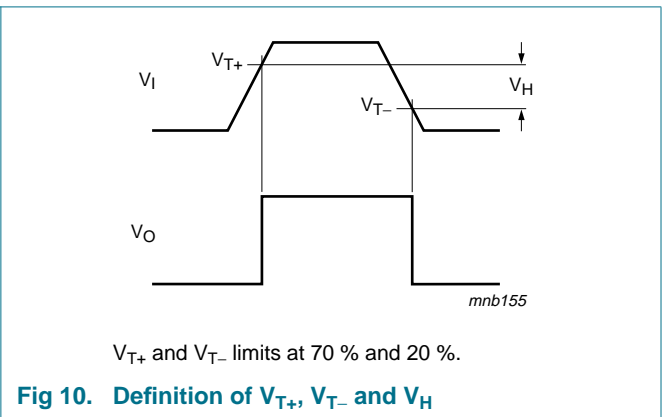
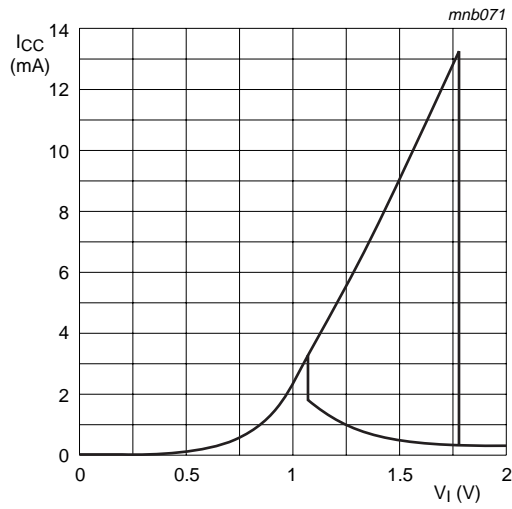
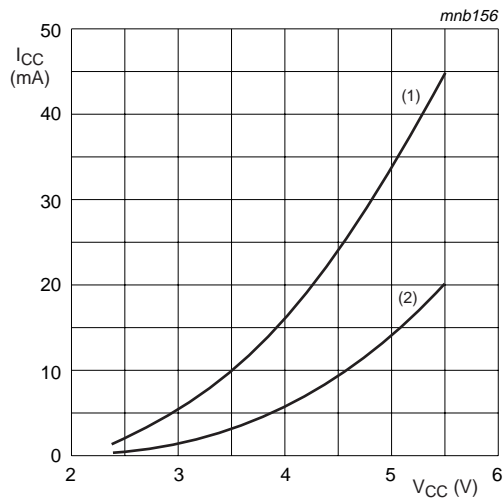


Fig 10. Definition of V_{T+}, V_{T-} and V_H



$V_{CC} = 3.0$ V.

Fig 11. Typical transfer characteristic



- (1) Positive-going edge.
- (2) Negative-going edge.

Linear change of V_I between 0.8 V to 2.0 V. All values given are typical unless otherwise specified.

Fig 12. Average I_{CC} as a function of V_{CC}

16. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

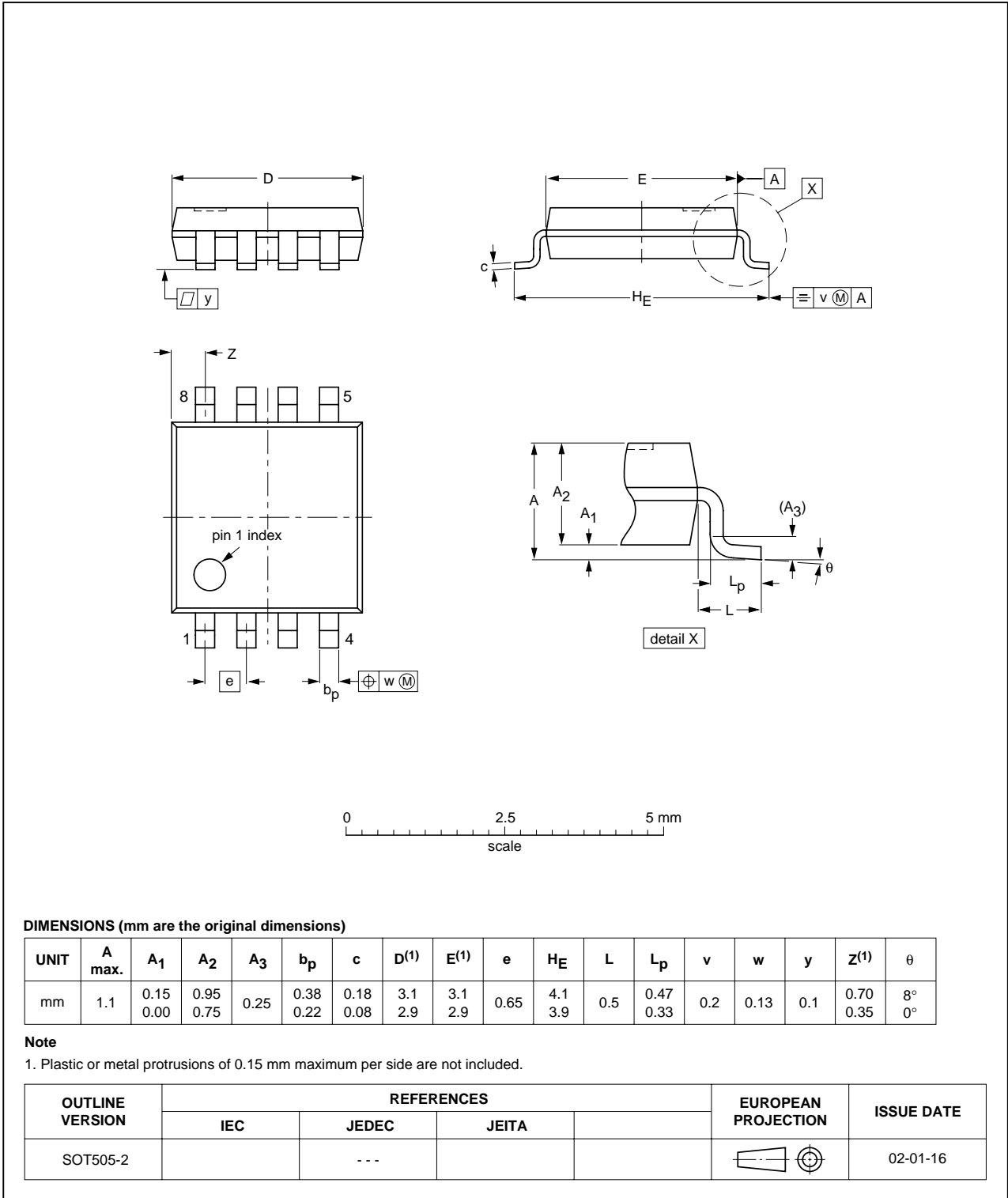


Fig 13. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

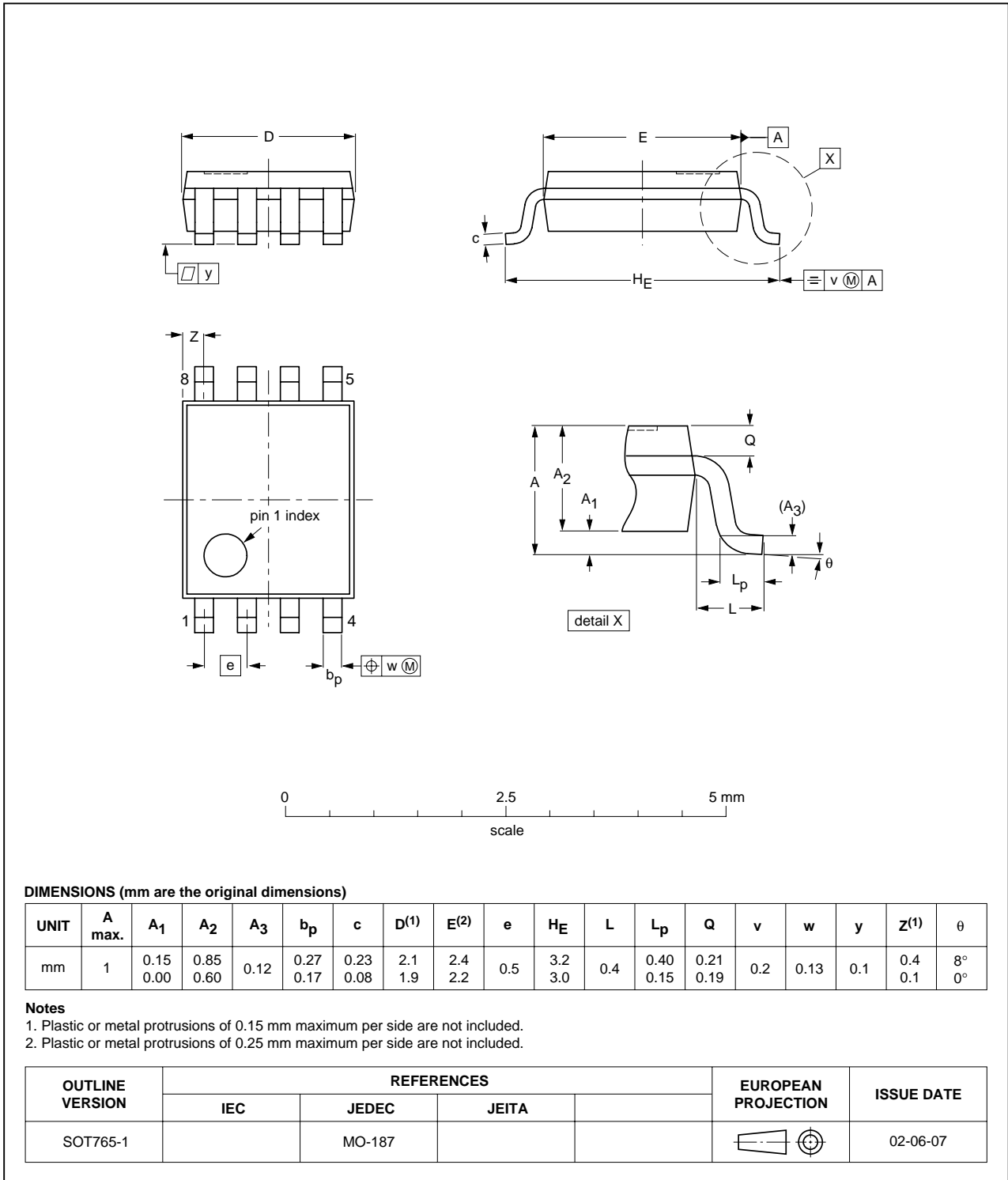


Fig 14. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

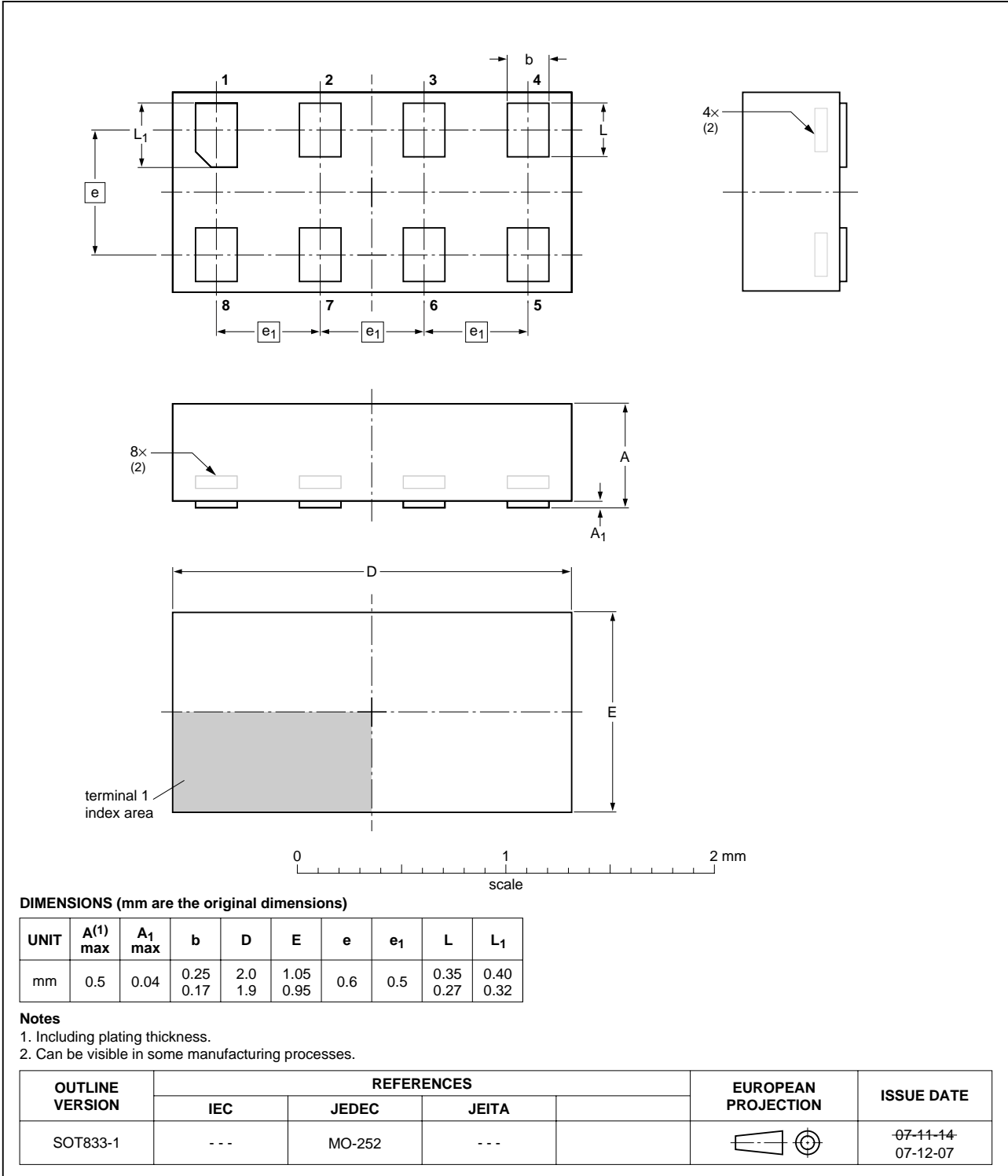


Fig 15. Package outline SOT833-1 (XSON8)

XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1

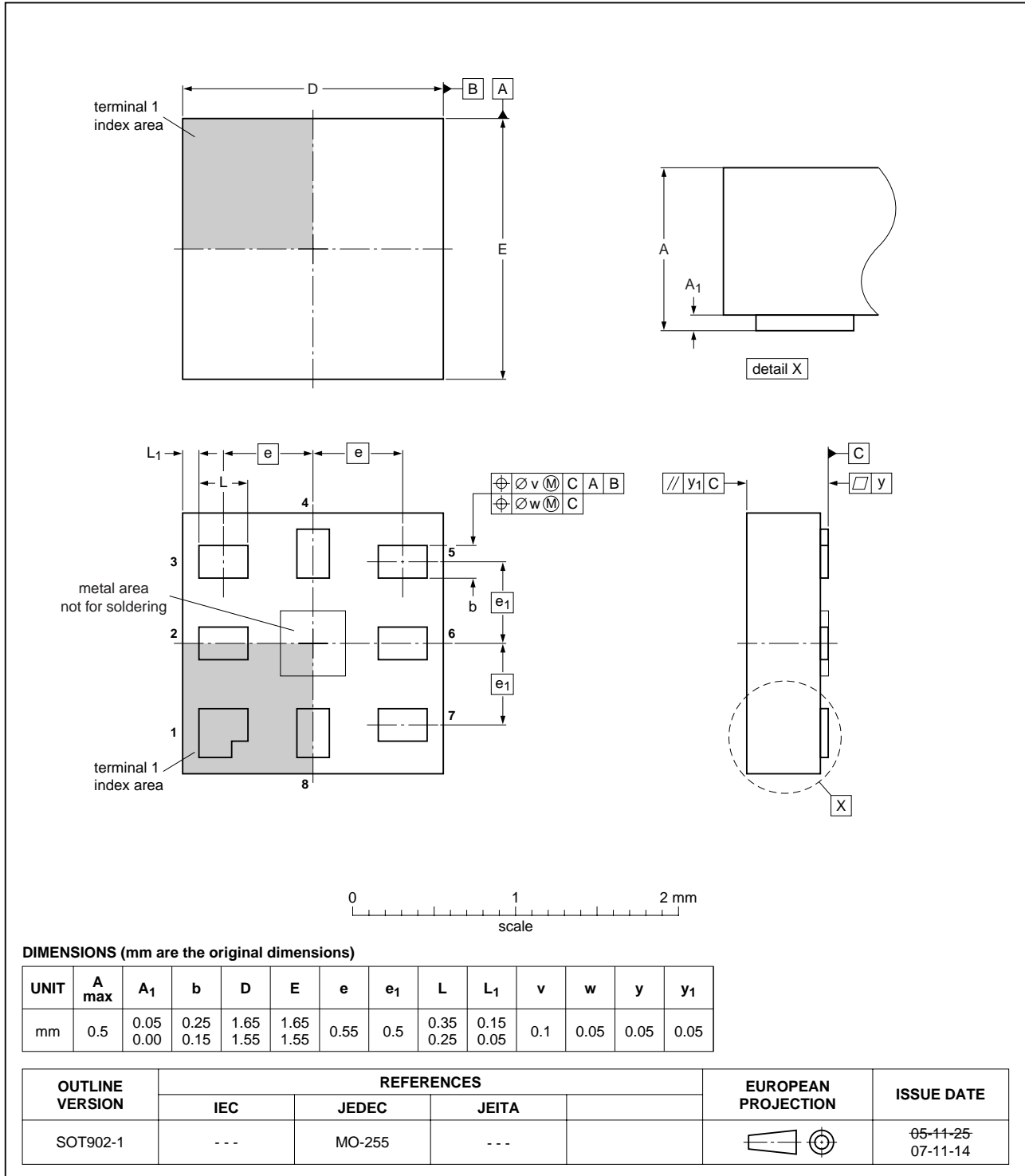


Fig 16. Package outline SOT902-1 (XQFN8U)

17. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

18. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC3G17_5	20080313	Product data sheet	-	74LVC3G17_4
Modifications:	<ul style="list-style-type: none"> • Figure 1 and Figure 2: pin numbers removed from logic symbols • Figure 16: package outline drawing updated to latest version 			
74LVC3G17_4	20070521	Product data sheet	-	74LVC3G17_3
74LVC3G17_3	20050131	Product data sheet	-	74LVC3G17_2
74LVC3G17_2	20041103	Product specification	-	74LVC3G17_1
74LVC3G17_1	20040624	Product specification	-	-

19. Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

19.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

20. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

21. Contents

1	General description	1
2	Features	1
3	Applications	1
4	Ordering information	2
5	Marking	2
6	Functional diagram	2
7	Pinning information	3
7.1	Pinning	3
7.2	Pin description	4
8	Functional description	4
9	Limiting values	4
10	Recommended operating conditions	5
11	Static characteristics	5
12	Dynamic characteristics	6
13	Waveforms	7
14	Transfer characteristics	9
15	Waveforms transfer characteristics	9
16	Package outline	11
17	Abbreviations	15
18	Revision history	15
19	Legal information	16
19.1	Data sheet status	16
19.2	Definitions	16
19.3	Disclaimers	16
19.4	Trademarks	16
20	Contact information	16
21	Contents	17

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 March 2008

Document identifier: 74LVC3G17_5